



(12) **United States Patent**
Tai et al.

(10) **Patent No.:** **US 9,144,490 B2**
(45) **Date of Patent:** **Sep. 29, 2015**

(54) **HIGH-LEAD COUNT IMPLANT DEVICE AND METHOD OF MAKING THE SAME**

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- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 63 days.

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(21) Appl. No.: **13/830,272**

(22) Filed: **Mar. 14, 2013**

(65) **Prior Publication Data**

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Related U.S. Application Data

- (60) Provisional application No. 61/640,569, filed on Apr. 30, 2012.

(51) **Int. Cl.**

H01B 13/00 (2006.01)
C23F 1/00 (2006.01)
A61F 2/14 (2006.01)
H01L 21/48 (2006.01)
H01L 23/498 (2006.01)
H01M 2/02 (2006.01)

(52) **U.S. Cl.**

CPC **A61F 2/14** (2013.01); **H01L 21/4846** (2013.01); **H01L 23/4985** (2013.01); **H01L 23/49894** (2013.01); **H01M 2/026** (2013.01)

(58) **Field of Classification Search**

USPC 216/2, 13, 58, 67; 438/706, 710
See application file for complete search history.

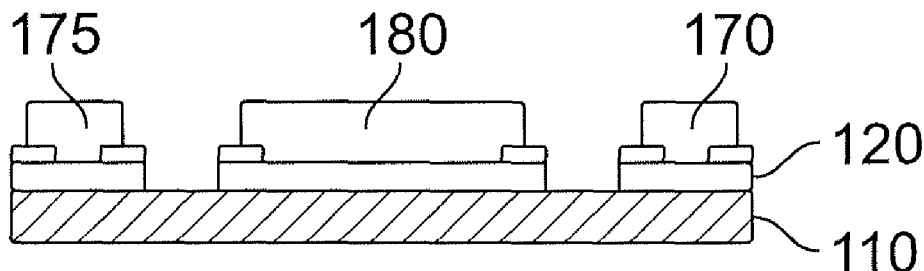
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(57) **ABSTRACT**

The invention provides chip packaging and processes for the assembly of retinal prosthesis devices. Advantageously, photo-patternable adhesive or epoxy such as photoresist is used as glue to attach a chip to the targeted thin-film (e.g., parylene) substrate so that the chip is used as an attachment to prevent delamination.

20 Claims, 17 Drawing Sheets



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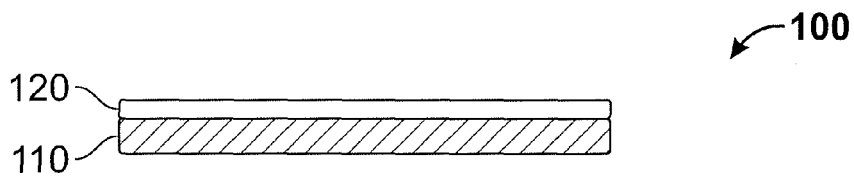


FIG. 1A

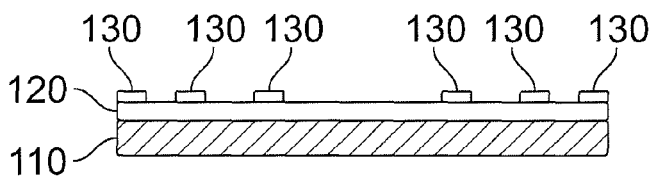


FIG. 1B

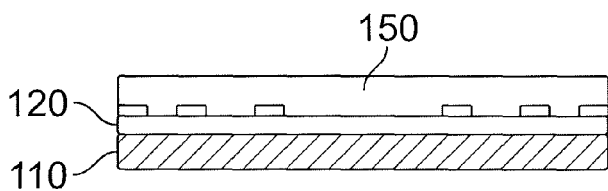


FIG. 1C

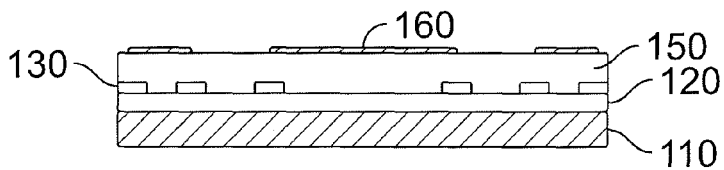


FIG. 1D

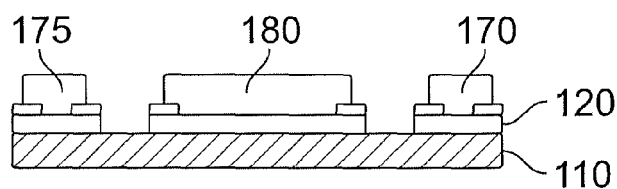


FIG. 1E

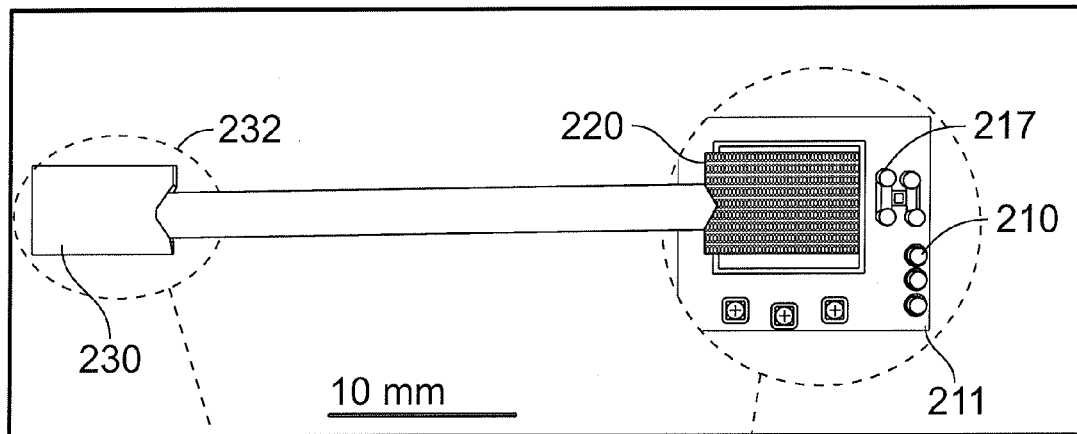


FIG. 2A

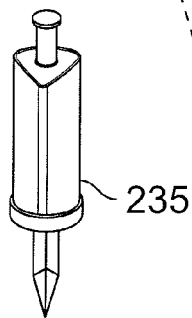


FIG. 2D

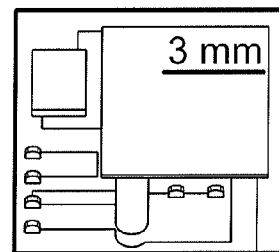


FIG. 2B

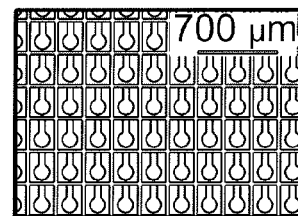


FIG. 2C

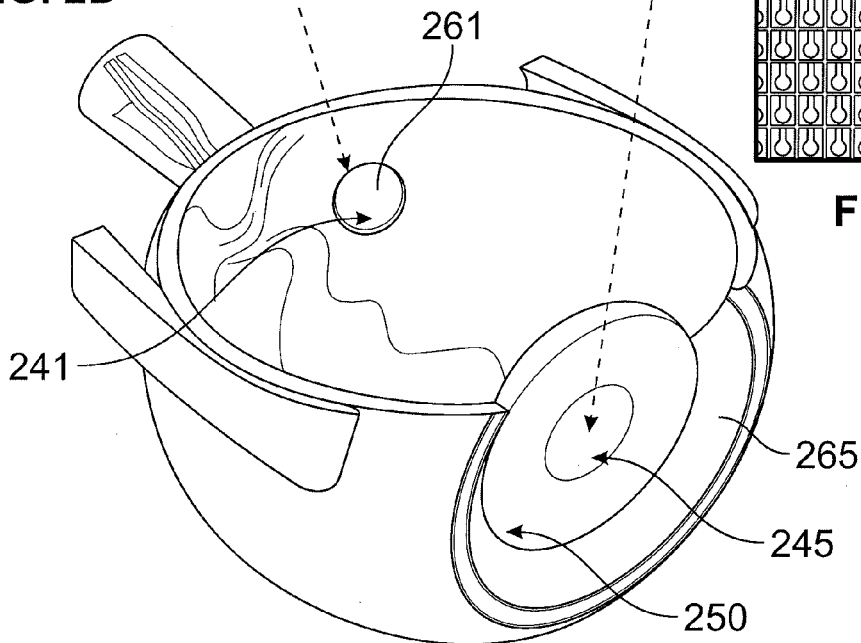


FIG. 2E

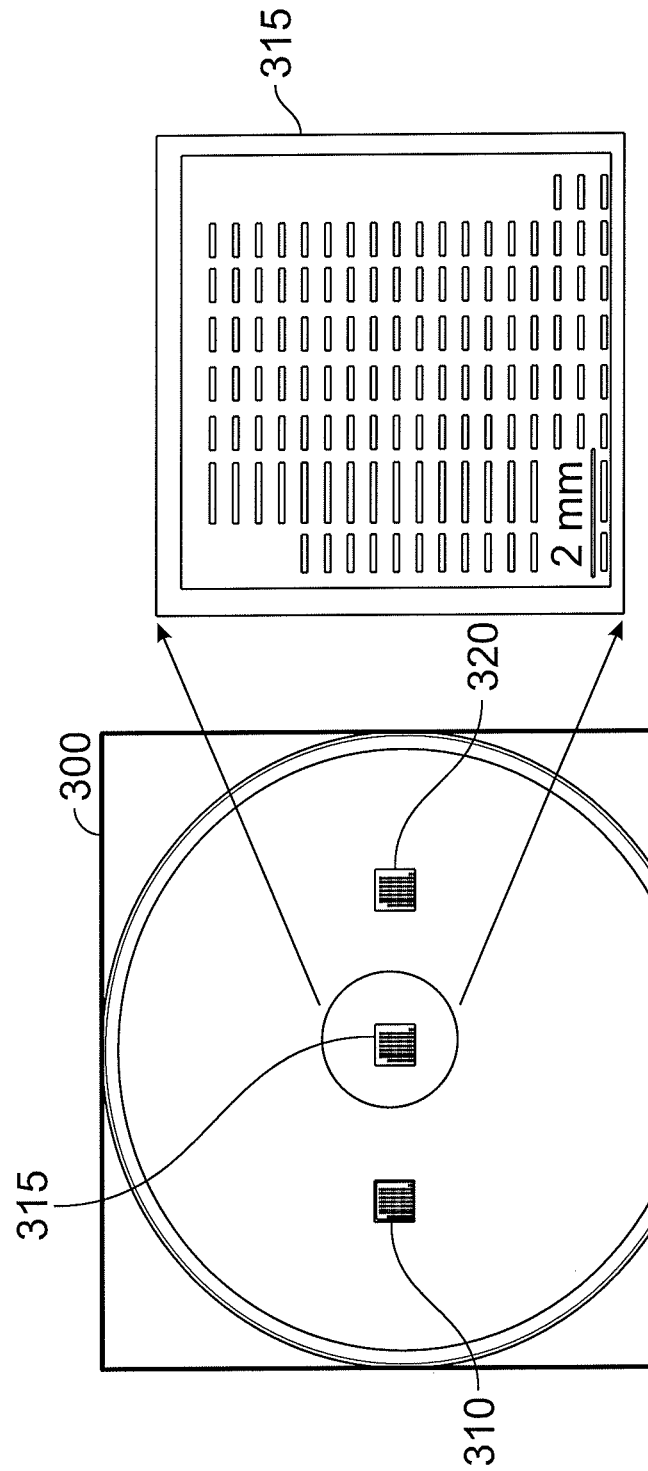


FIG. 3B

FIG. 3A

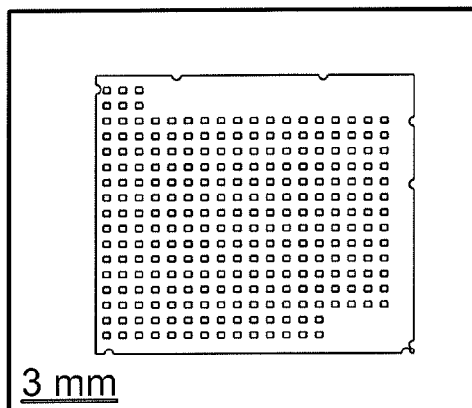


FIG. 4A

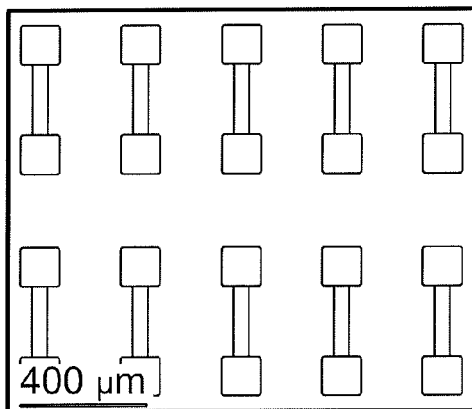


FIG. 4B

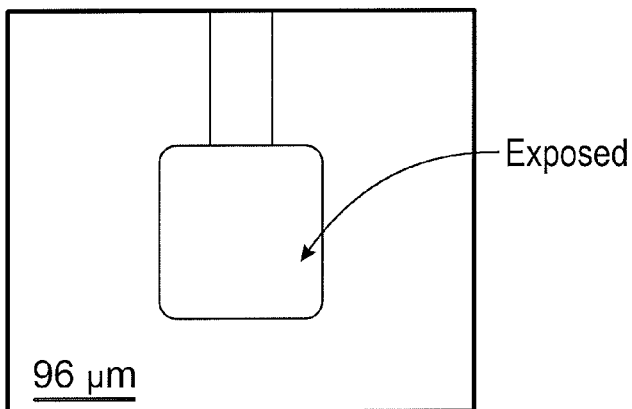


FIG. 4C

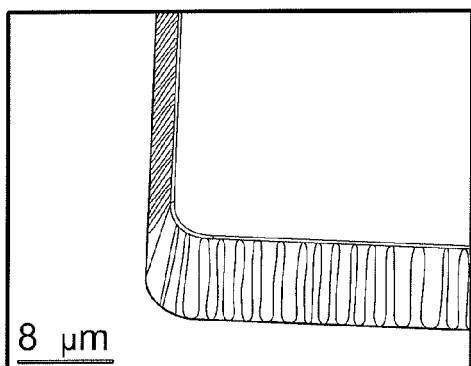


FIG. 5A

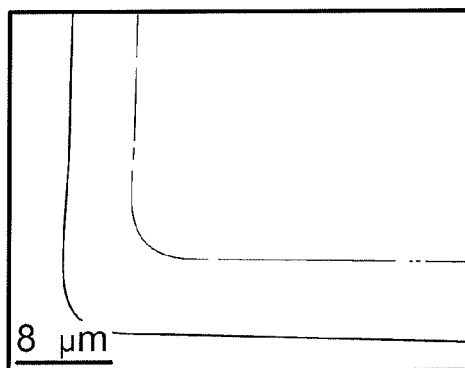


FIG. 5B

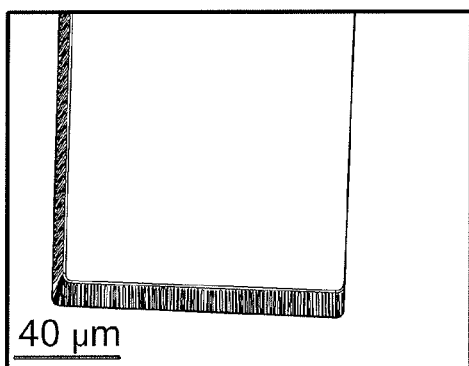


FIG. 5C

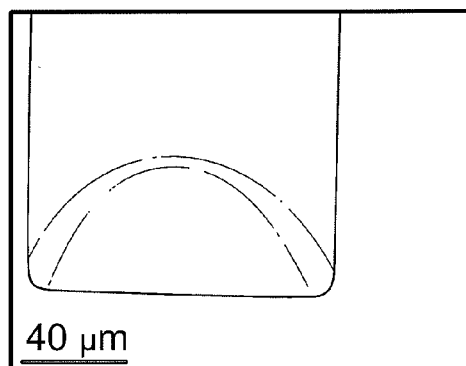


FIG. 5D

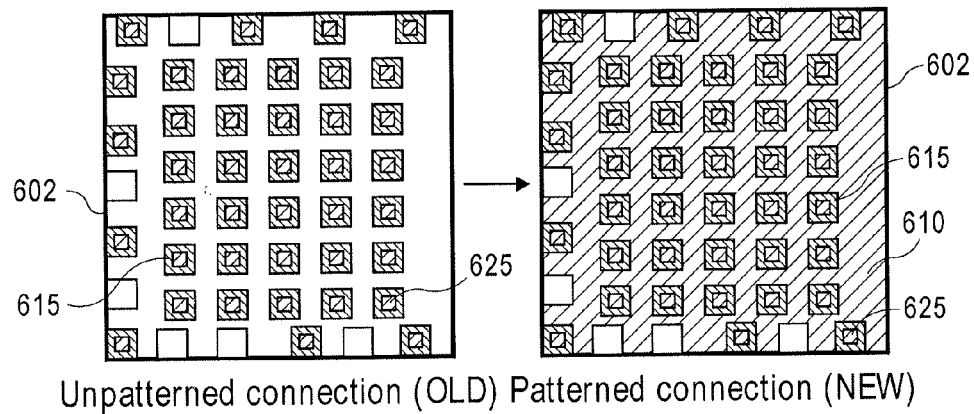


FIG. 6A

FIG. 6B

LEGEND

Chip

Metal pads

Conductive epoxy:
2% of total area

Patterned area: 92%
of the total area

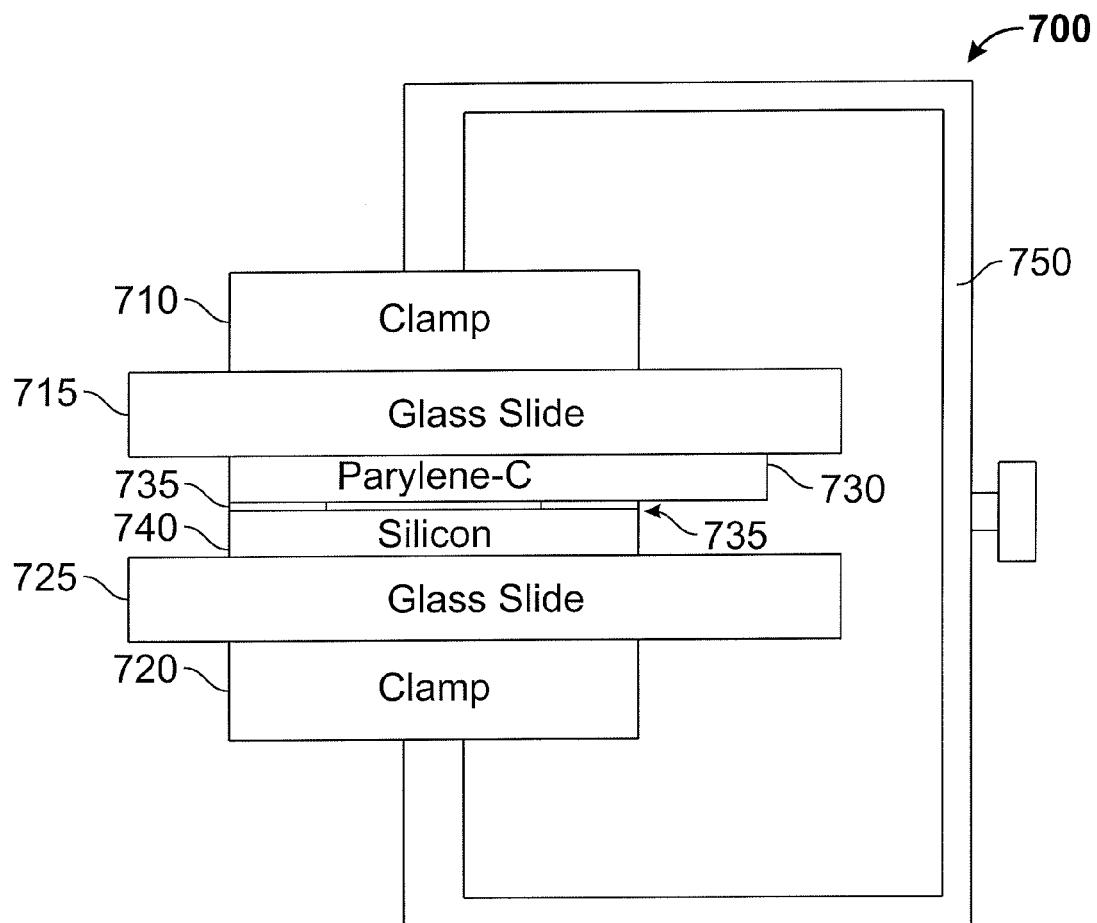
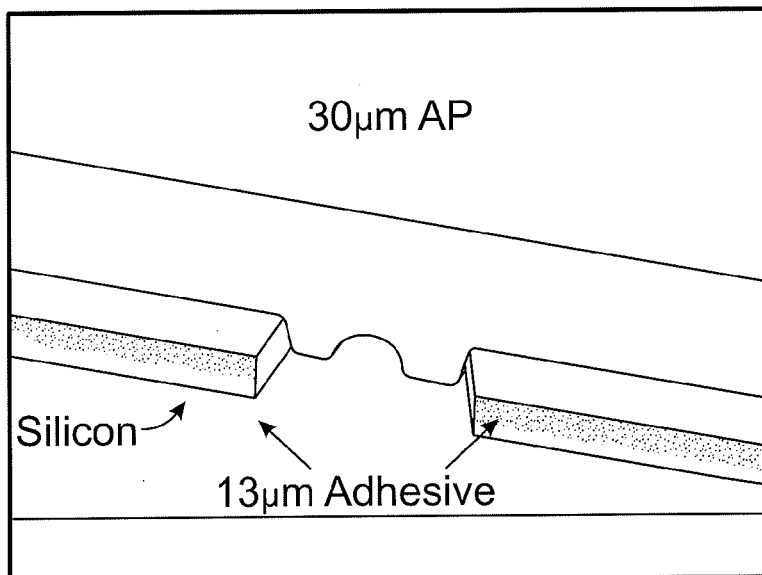
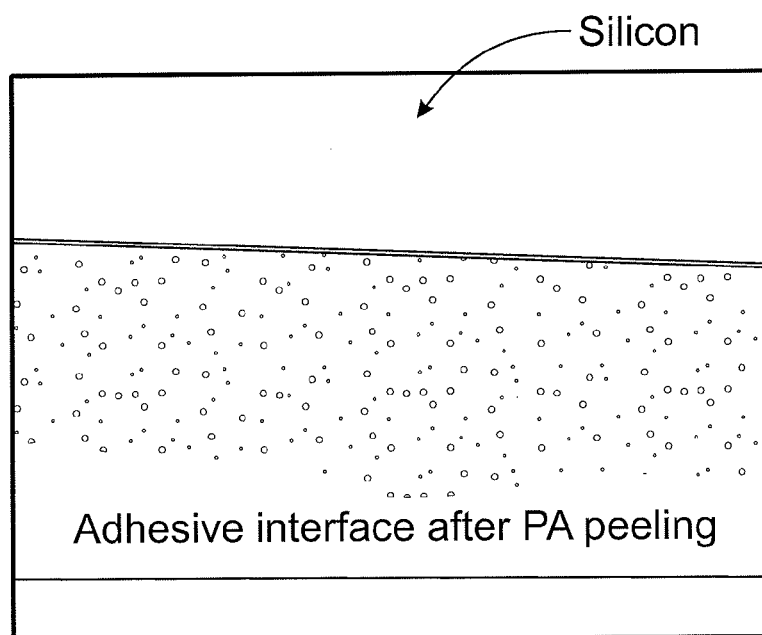


FIG. 7

**FIG. 8A****FIG. 8B**

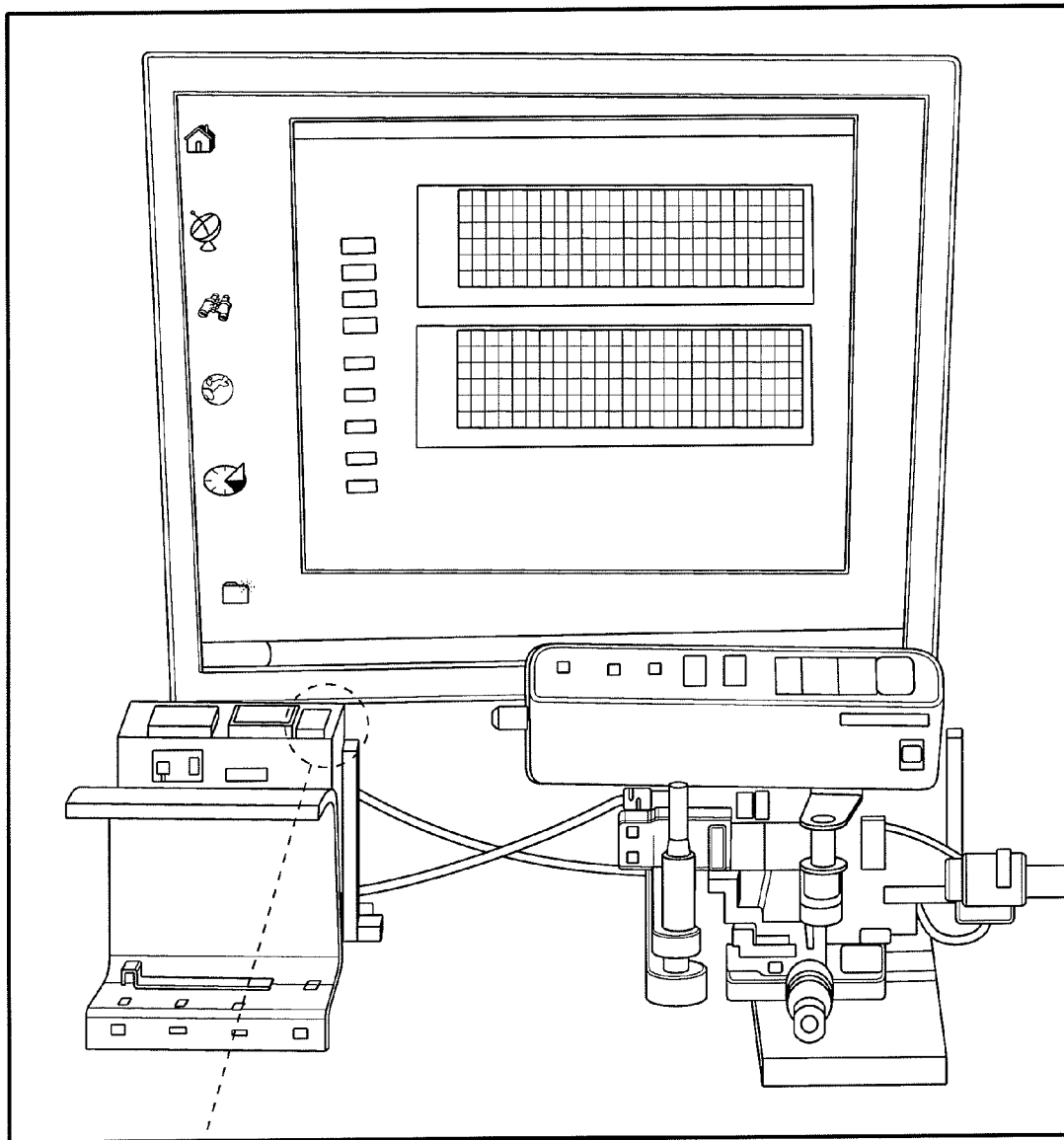


FIG. 9A

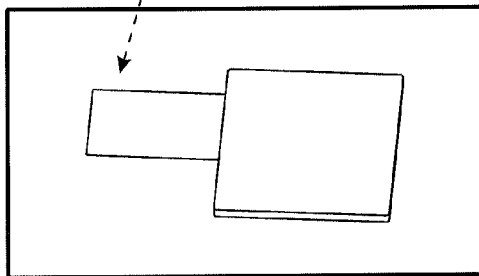


FIG. 9B

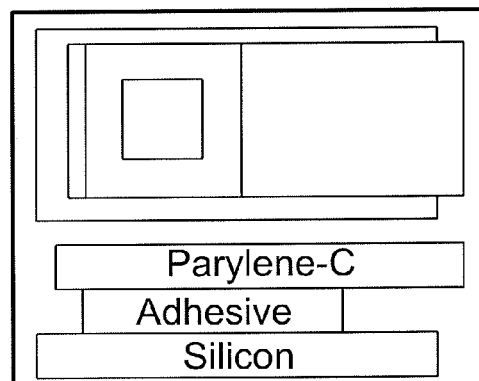


FIG. 9C

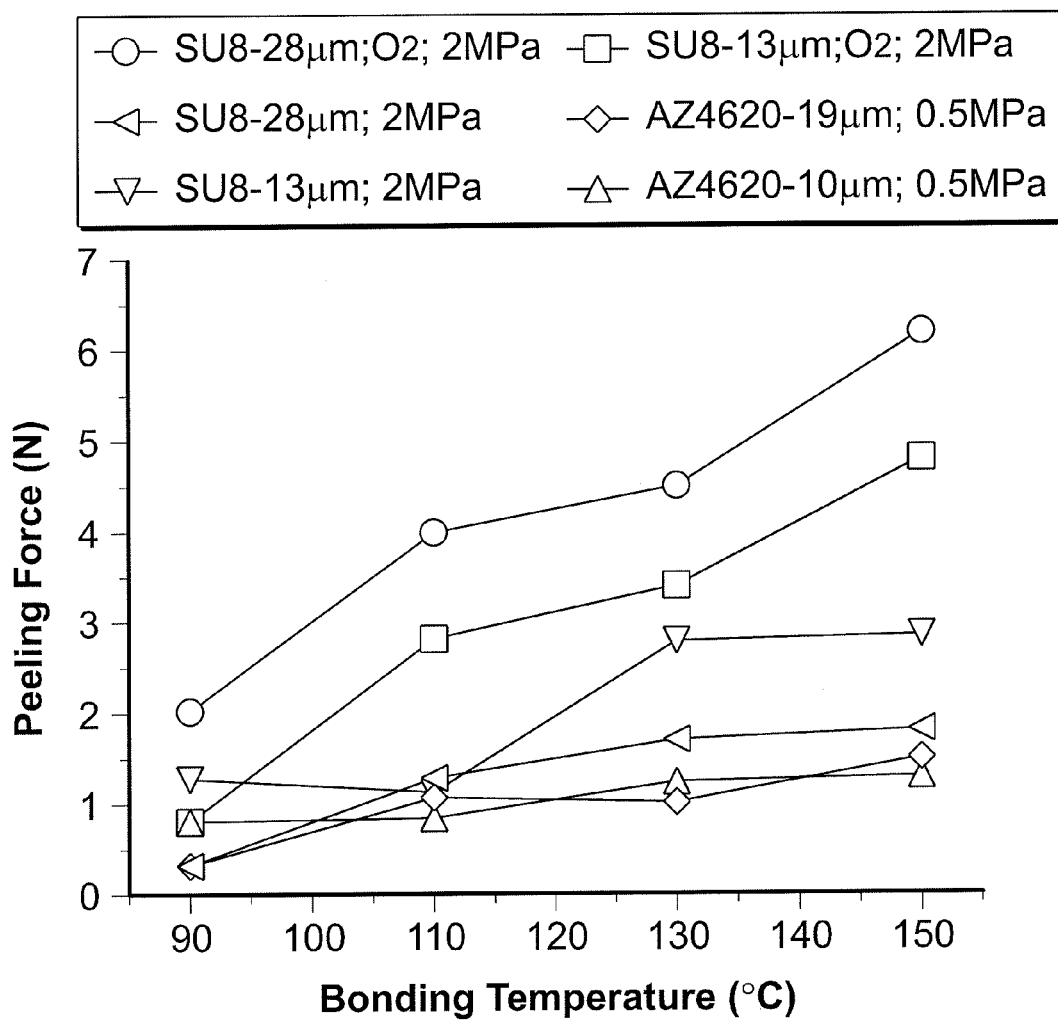


FIG. 10

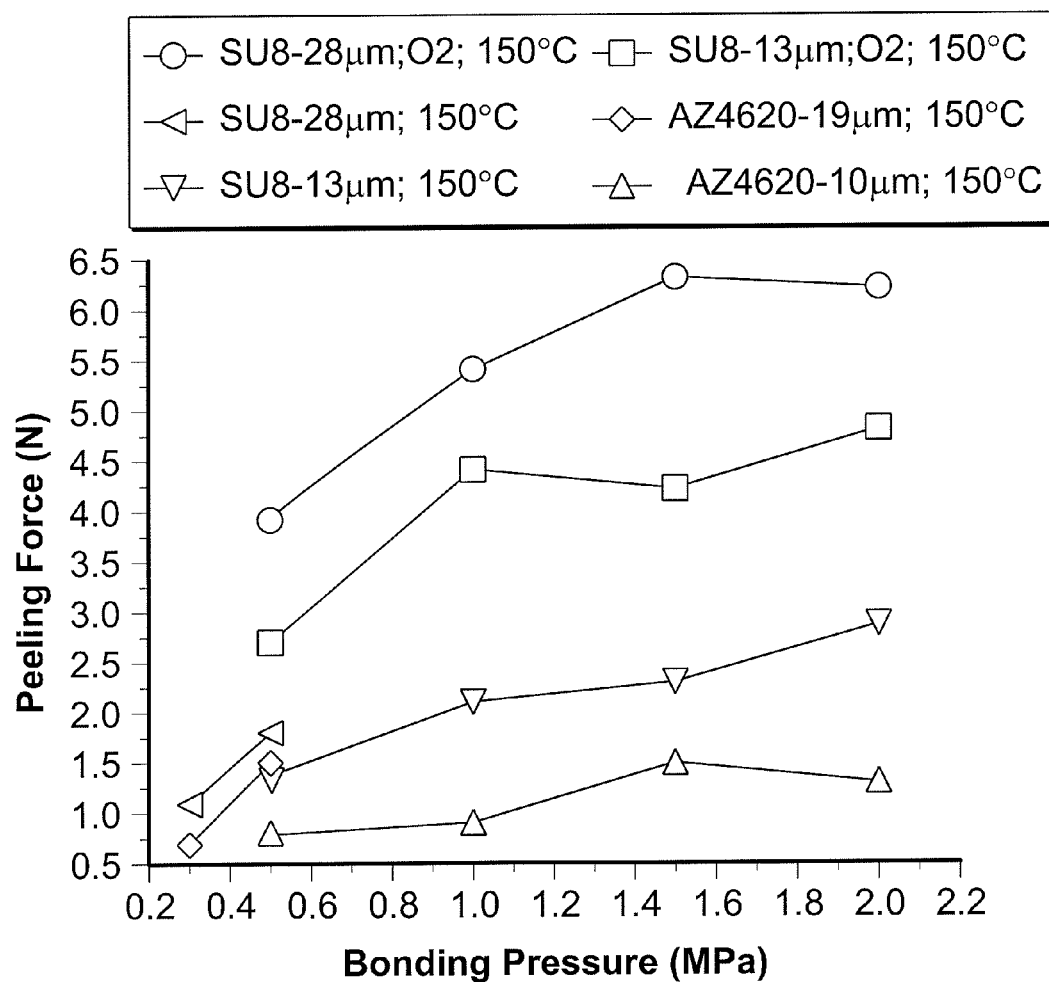


FIG. 11

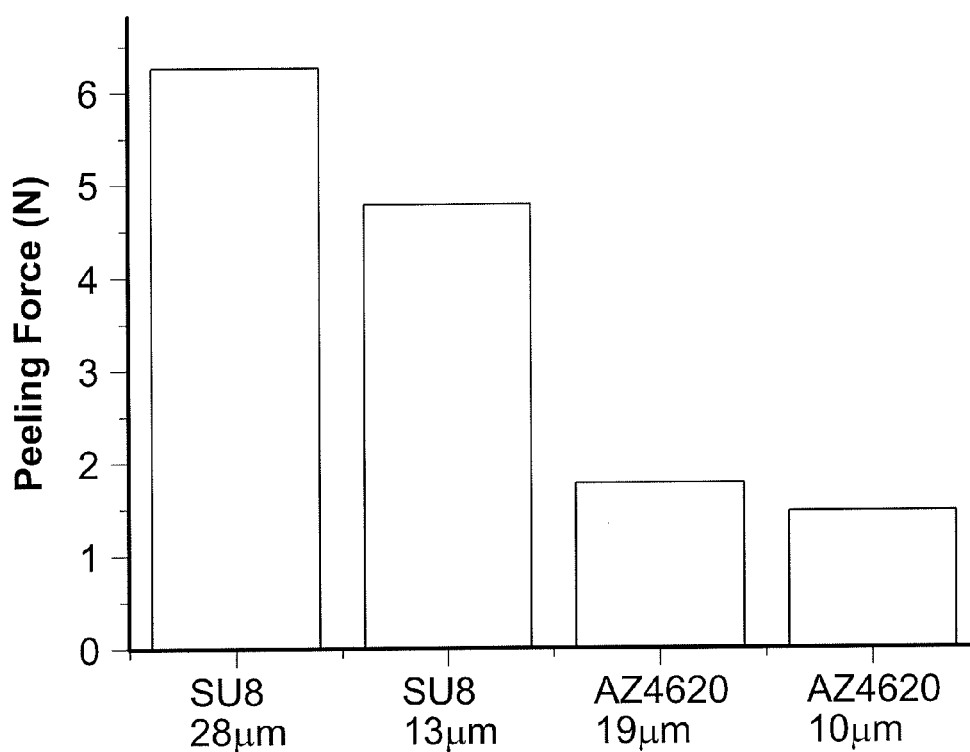


FIG. 12A

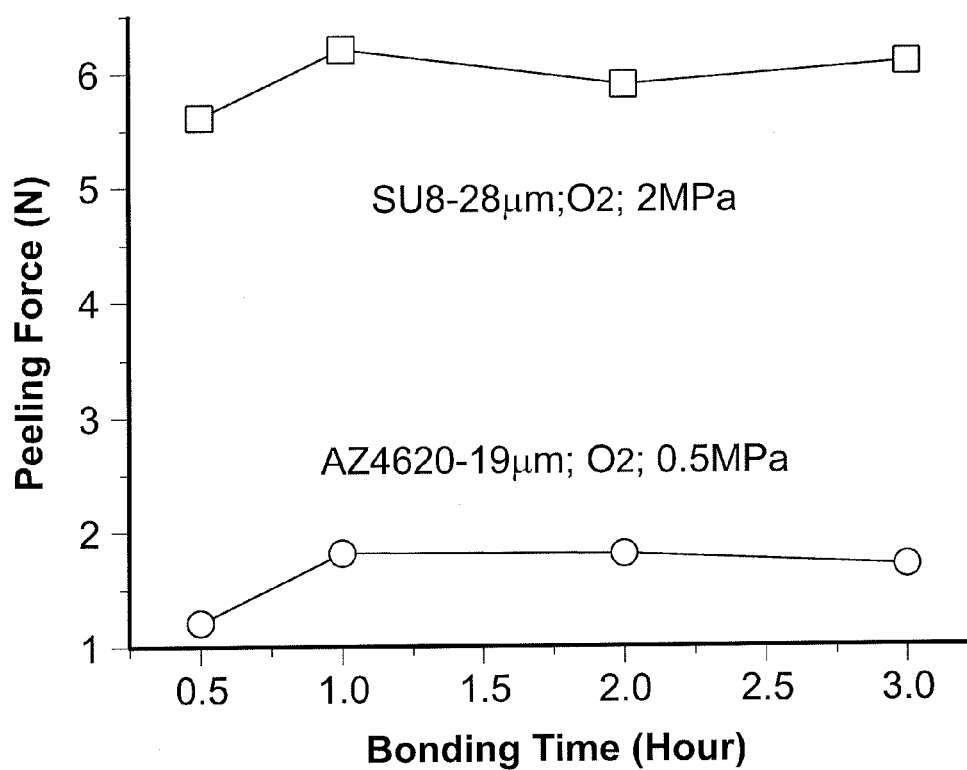


FIG. 12B

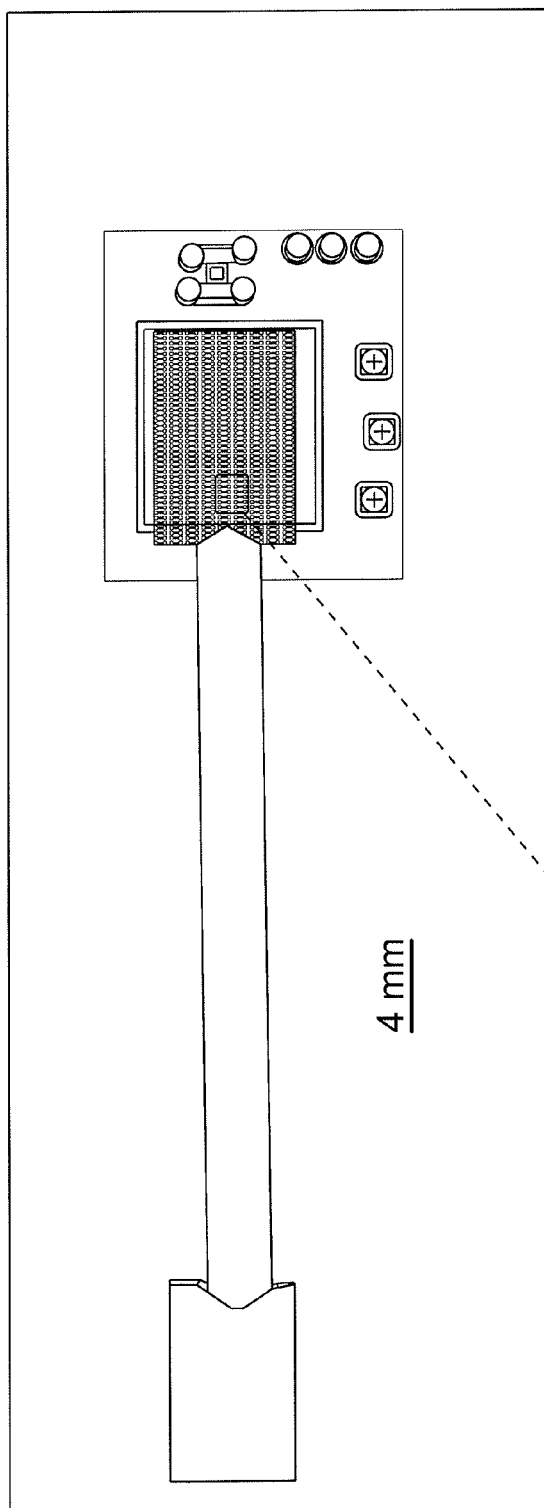


FIG. 13A

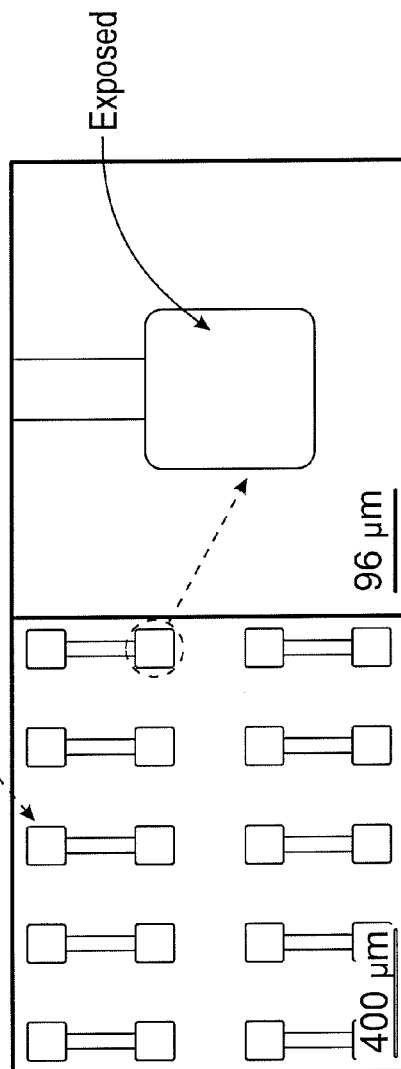


FIG. 13C

FIG. 13B

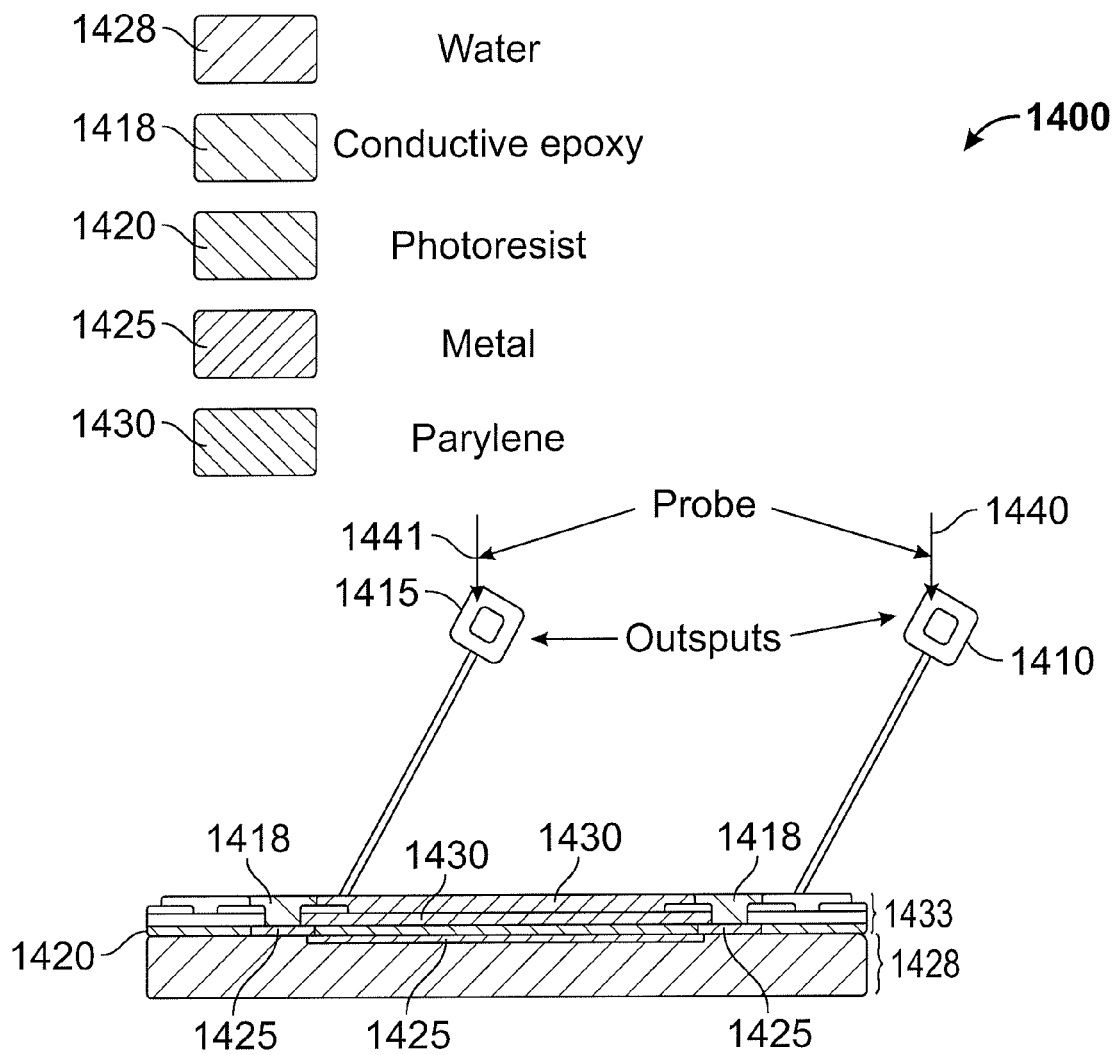


FIG. 14

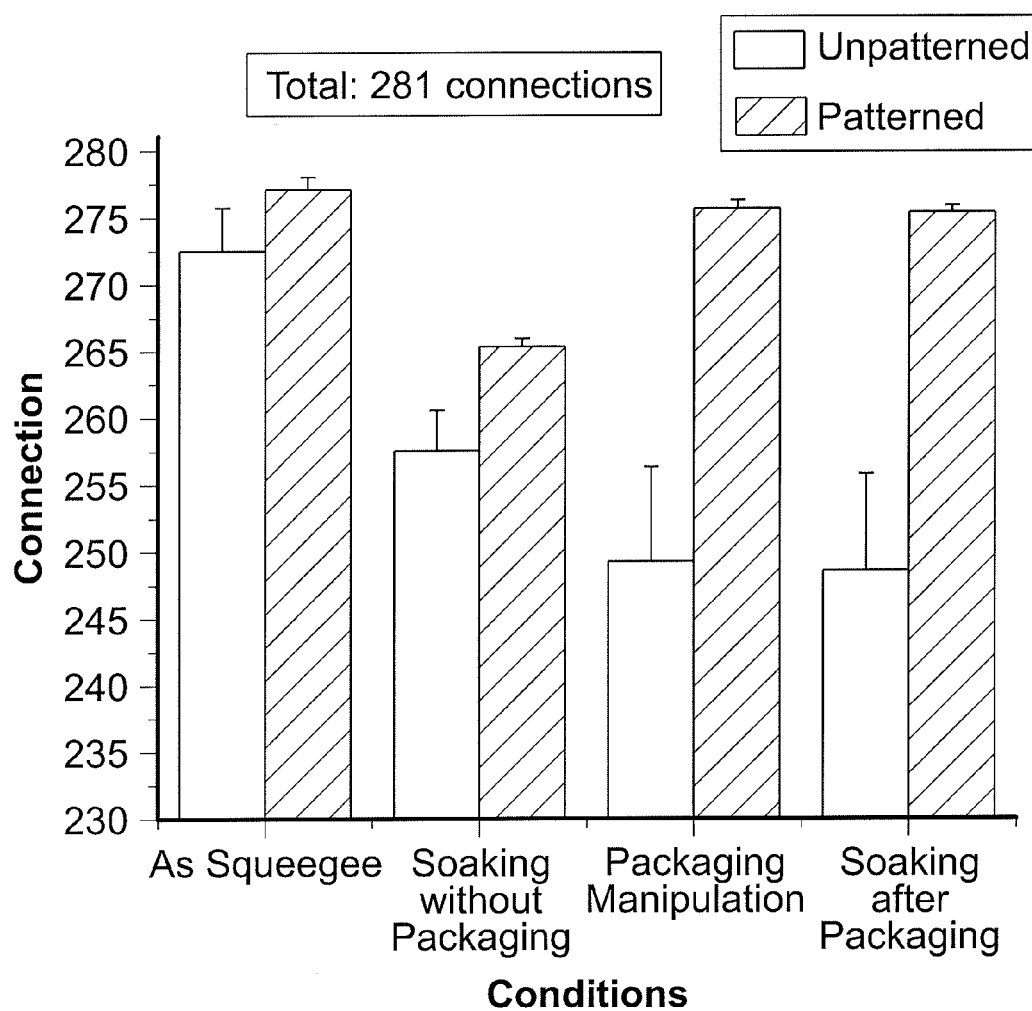
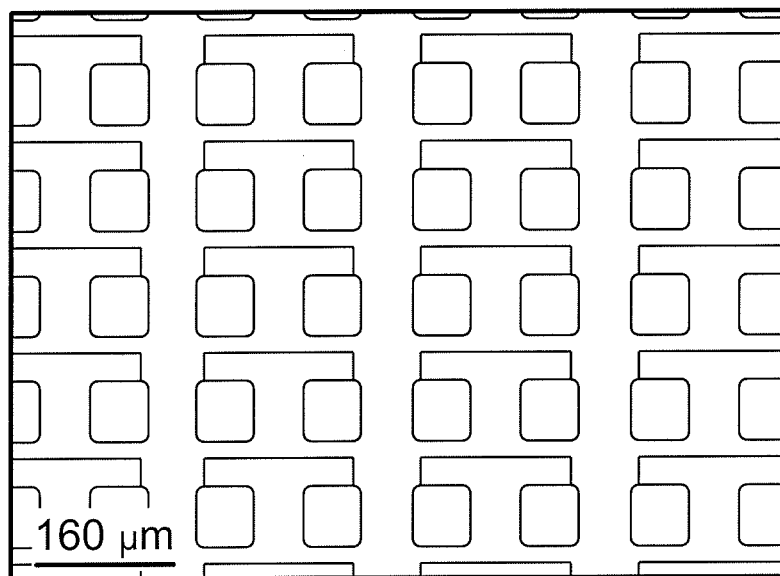
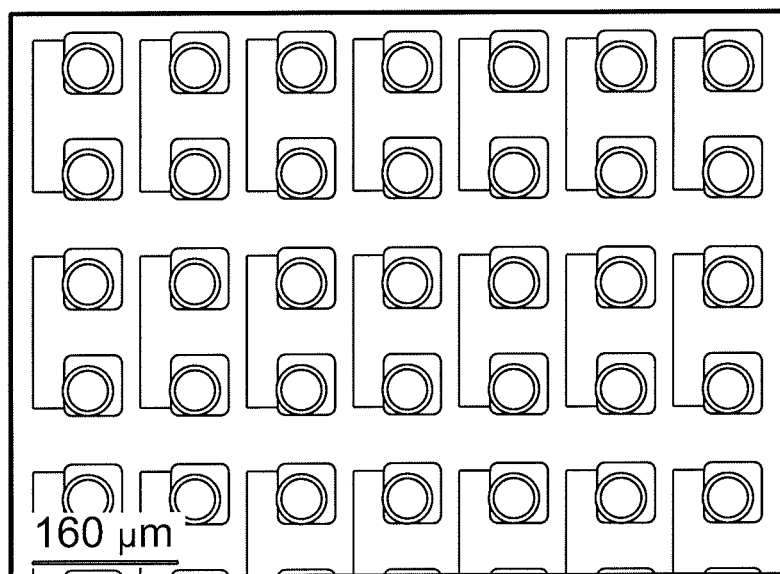


FIG. 15

**FIG. 16A****FIG. 16B**

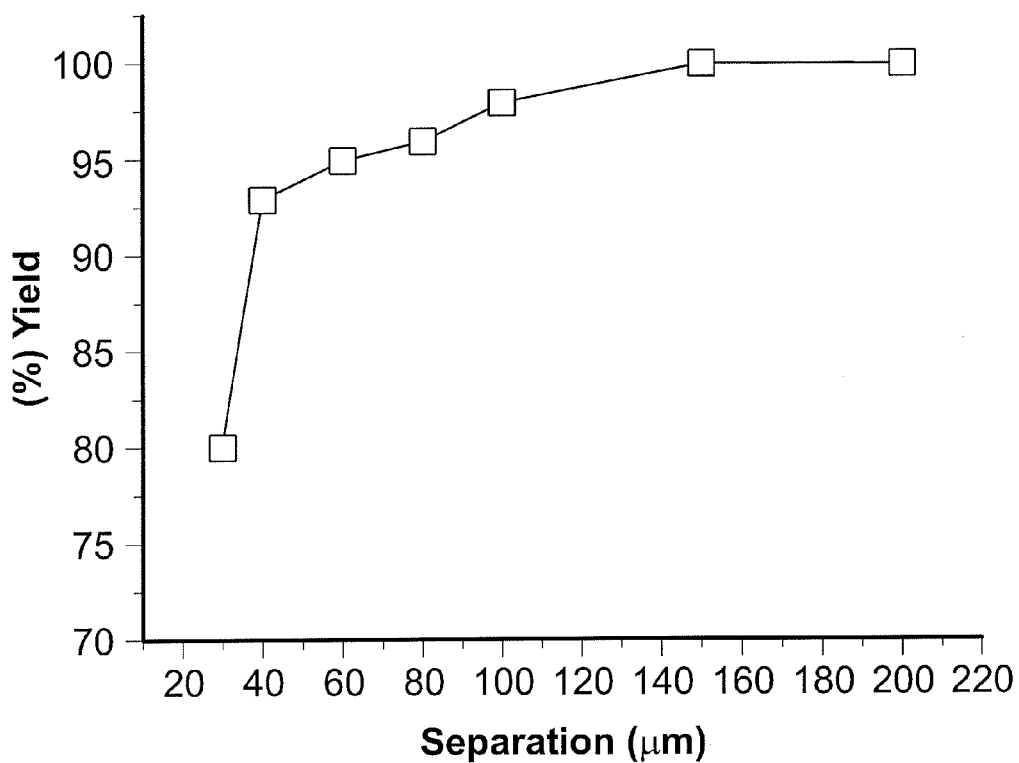


FIG. 16C

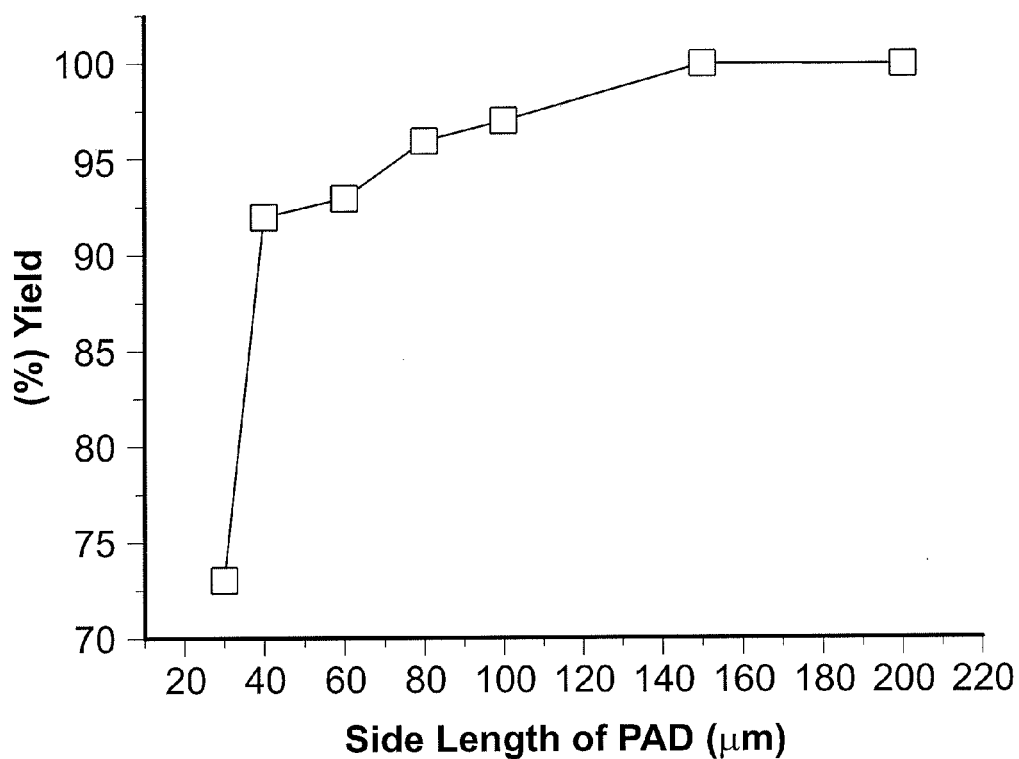


FIG. 16D

1

HIGH-LEAD COUNT IMPLANT DEVICE AND METHOD OF MAKING THE SAME

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority to U.S. patent application Ser. No. 61/640,569, filed Apr. 30, 2012, the disclosure of which is hereby incorporated by reference in its entirety for all purposes.

STATEMENT AS TO RIGHTS TO INVENTIONS MADE UNDER FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

This invention was made with government support under EEC0310723 awarded by the National Science Foundation. The government has certain rights in the invention.

FIELD OF INVENTION

This invention relates to biomedical implants in general and in particular to biomedical implants that employ a parylene substrate that allows the total connection and fabrication of a biomedical implant comprising semiconductor chips or other pre-manufactured electrical components such as transistors, resistors, capacitors or inductors.

BACKGROUND OF THE INVENTION

One of the biggest challenges that a prosthetic implant has to overcome is the reliable packaging of integrated circuit (IC) chips with bio-devices to withstand corrosive body fluids. This is especially true for complex neural implants and retinal implants because hundreds of or thousands of electrodes may be needed to be connected to the necessary IC chips (see, K. D. Wise et al., *International Conference of the Engineering in Medicine and Biology Society on Neural Engineering* 2007, pp. 398-401). In comparison, a pacemaker has only one stimulating channel and a cochlear implant requires only 5 to 6 stimulating electrodes to be able to regain hearing capabilities of an impaired patient (see, K. Najafi et al., *IEEE Conference on Nano/Micro Engineered and Molecular Systems*, 2004, pp. 76-97). In addition, in order to avoid possible infection and medical complications, it is desirable to have prosthetic devices completely inside a subject's body. This means that technologies for integration, connection and packaging of IC chips for high-lead-count implant devices are of high demand. As shown previously, aligned electrical connection can be done between parylene-C interfaces and high density multi-channel chips by a conductive epoxy squeegee technique (see, Jay H. C. Chang, Ray Huang, and Y. C. Tai, *Proc. TRANSDUCERS* 2011, pp. 378-381), where a PDMS mold was used to house the IC chips and serve as the safety squeegee buffer zone. However, it is too big to be implanted inside a human eyeball (<1-2 cm³) (see, M. Humayun et al., *Vision Research*, 43 (2003), pp. 2573-2581). In addition, since the adhesion only relied on conductive epoxy contacting less than 2% of the total connection area, delamination could easily happen when even a small force was applied to the assembled devices. This would be especially serious during surgery. Since the next generation intraocular retinal prosthetics require the whole device, including coils, electrodes, stimulation chip and other ASICs to be fitted inside a human eyeball, the device must be further designed in terms of both size and surgical complexity.

2

Parylene-C has become a popular material for BioMEMS implant applications due to its superior properties (see, J. H. Chang et al, *Proc. TRANSDUCERS* 2011, pp. 390-393; J. H. Chang et al, *Proc. NEMS* 2011, pp. 1067-1070). It has also served as an intermediate layer for silicon wafer bonding (see, H. Noh et al, *J Micromech. Microeng.* 14(2004), 625; H. Kim et al., *J. Microelectromech. Syst.* 14(2005), 1347-1355). However, the bonding between parylene-C and silicon is still problematic.

There are various processes for packaging integrated circuit (IC) dice. Some packaging techniques contemplate the creation of electronic modules that incorporate multiple electronic devices (e.g. integrated circuits, passive components such as inductors, capacitor, or resistors) into a single package. Despite the advances of the prior art, and although implantable devices have been developed with micro-electrical-mechanical system (MEMS) technology, there is a need for better packaging technology, especially for high-lead-count retinal and neural implants. The present invention provides these and other needs.

BRIEF SUMMARY OF THE INVENTION

The present invention provides substrates, methods and processes to assemble IC chips to thin-film substrates such as a parylene substrates for medical implants such as retinal implants. Advantageously, the inventive packaging technology can be used to produce 10,000 or more connections within an area as small as 36 mm², a chip size reasonable for retinal implants. The current invention provides methods for improving packaging techniques.

As such, in one embodiment, the present invention provides a method for fabricating a thin-film substrate such as a parylene substrate for attachment of a device, comprising: depositing a first thin-film layer such as a parylene layer on a silicon-wafer to form a bottom thin-film layer; depositing a metal to the bottom parylene layer to form an electrical connection; depositing a second thin-film layer such as parylene layer adjacent to the metal to form a top thin-film layer and a thin-film metal thin-film sandwich (e.g., parylene-metal-parylene sandwich); providing a mask adjacent to the top thin-film layer; and directing an etching beam onto the mask to fabricate the thin-film substrate (e.g., parylene substrate) for attachment of the device.

In another embodiment, the present invention provides the thin-film substrate (e.g., parylene substrate) made by the inventive process. The substrate is useful to integrate, connect and package IC chips for high-lead-count implant devices.

In order to validate this technology, chips designed with 268 connections to mimic real IC chips under development were used for the measurement of connection yield. In addition, after squeegee connection and encapsulation by a thick parylene-C coating, the connected chips underwent accelerated soaking tests in a high temperature saline solution. The results show that the technique provides exceptionally high connection yield.

In yet another embodiment, the present invention provides a method for assembling an integrated circuit to a thin-film substrate (e.g., parylene substrate), comprising:

spin coating a photo-patternable adhesive or epoxy to an integrated circuit (IC) to form a covered IC; masking the covered IC; and patterning the covered IC using photolithography to expose a plurality of bonding pads on the IC chip to form a patterned IC to integrate into the thin-film substrate (e.g., parylene substrate).

In still another embodiment, the present invention provides a biocompatible thin-film (e.g., parylene) substrate for attachment of a device, comprising:

- a first thin-film (e.g., parylene) layer;
- a metal adjacent to the first thin-film layer;
- a second thin-film (e.g., parylene) layer adjacent to the metal to form a thin-film metal thin-film sandwich (e.g., parylene-metal-parylene sandwich), wherein the second layer of thin-film has an opening, the opening having at least one electrical contact provided on an internal surface thereof, the opening configured to accept at least one electrical circuit device and to provide electrical communication between the at least one electrical contact and the at least one electrical circuit device, the biocompatible thin-film (e.g., parylene) substrate configured to be implanted within a living organism after accepting the at least one electrical circuit device.

In certain aspects, the device having at least one electrical circuit is an integrated circuit (IC) chip. In addition, in one aspect the device such as an IC chip is integrated into the substrate by a conductive epoxy squeegee electrical connection. Preferably, the device is integrated into the substrate by a photo-patternable adhesive or photoresist used as a mechanical glue.

These and other aspects, objects, and embodiments will become more apparent when read with the detailed description and figures which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A-E show a fabrication process of a flexible parylene-C connection substrate according to one embodiment of the present invention.

FIG. 2 A-E show in FIG. 2A a schematic representation of the fabricated flexible parylene-C substrate connected with a chip and discrete component. FIG. 2B shows the backside of the discrete component area. FIG. 2C shows a close-up view of the chip integration; FIG. 2D shows a retinal tack; FIG. 2E shows a schematic of an eye and integration of a fabricated flexible parylene-C substrate connected with a chip.

FIG. 3A-B show a custom holder for chip assembly technique.

FIG. 4 A-C show in FIG. 4A a dummy chip for assembly yield test; FIG. 4B-C show pads also served as alignment marks.

FIG. 5 A-D show in FIG. 5A unbaked AZ4620; FIG. 5B shows AZ4620 baked at 140° C. for 30 minutes in a vacuum oven; FIG. 5C and FIG. 5D show the slope formed by reflow is beneficial for conductive epoxy to be fed through.

FIG. 6A-B show the gluing area was about 2% as is shown in FIG. 6A; FIG. 6B shows the gluing area increased to about 94% (2%+92%) by the extra photoresist used as glue.

FIG. 7 shows a schematic representation of a clamp as the bonding tool on the testing samples.

FIG. 8 A-B show in FIG. 8A a cross-sectional SEM image of the bonding (2 MPa, 130° C.); FIG. 8B shows the adhesive interface after parylene peeling.

FIG. 9A-C show in FIG. 9A the setup of the force gauge to measure the peeling force. FIG. 9B shows a real testing sample after bonding; FIG. 9C shows the schematic representation of the testing sample.

FIG. 10 shows the peeling force vs bonding temperature for various photo-patternable adhesives.

FIG. 11 shows the peeling force vs bonding pressure for various photo-patternable adhesives.

FIG. 12A-B shows in FIG. 12A the maximum peeling forces of different photo-patternable adhesives; FIG. 12B shows the peeling force vs bonding time for different photo-patternable adhesives.

FIG. 13A-C show in FIG. 13A a surgical parylene-C device connected with silicon chip and discrete components; FIG. 13B and FIG. 13C show metal pads are exposed with other area covered by adhesives.

FIG. 14 shows the setup of the measurement, wherein the electrode array outputs (the electrode end that is placed on macula) were probed to check the connection.

FIG. 15 shows the connection yields under 4 different conditions; reliability tests were carried out after squeegee connection, encapsulation by parylene-C coating, and accelerated soaking in 90° C. saline.

FIG. 16A-D show in FIG. 16A dummy chips with 40 μm by 40 μm pad size and 40 μm separation; FIG. 16B shows the connection between a parylene substrate and dummy chip; FIG. 16C shows the yield vs separation of pads; FIG. 16D shows the yield vs side length of pads.

DETAILED DESCRIPTION OF THE INVENTION

I. Embodiments

The present invention relates to biomedical implants in general and in particular to biomedical implants that employ a thin-film (e.g., parylene) substrate that allows the total connection and fabrication of a biomedical implant comprising semiconductor chips and/or other pre-manufactured electrical components. In one embodiment, the present invention provides a method for fabricating a thin-film substrate such as a parylene substrate for attachment of a device, comprising:

- depositing a first thin-film layer such as a first parylene layer on a silicon-wafer to form a bottom thin-film layer;
- depositing a metal to the bottom thin-film (e.g., parylene) layer to form an electrical connection;

- depositing a second thin-film layer such as second parylene layer adjacent to the metal to form a top thin-film layer and a thin-film metal thin-film sandwich (e.g., parylene-metal-parylene sandwich);

- providing a mask adjacent to the top thin-film layer; and
- directing an etching beam onto the mask to fabricate the thin-film substrate (e.g., parylene substrate) for attachment of the device. The first thin-film layer can be the same or different than the second thin-film layer. Although parylene is the preferred substrate, a skilled artisan will appreciate that the material can be other thin-film polymers such as polyimide, Teflon, kapton, or a printed circuit board (PCB) and the like. The remainder of the application will use parylene as an illustrated example. Other thin-films can also be used.

In certain aspects, the present invention provides a fabrication process 100 for a parylene-substrate, such as a flexible parylene-C substrate. In one exemplary embodiment, FIG. 1A shows a 5 μm first parylene-C layer (bottom layer) 120 deposited on a silicon substrate 110 such as a HMDS treated silicon wafer, which aids in the device being detached such as being released in distilled or deionized water, preferably deionized water.

Next, as is shown in FIG. 1B, adjacent to the first parylene layer 120 (bottom parylene layer) is a metal 130 such as a titanium/gold (Ti/Au) alloy for a metal lift-off. The metal provides an electrical connection. A second parylene layer 150 (top layer) such as a thicker parylene-C (about 40 μm) layer is then deposited to complete the parylene-metal-parylene sandwich structure as is shown in FIG. 1C. The

5

process includes providing a mask **160** such as a metal mask (e.g., aluminum) deposited as a parylene-C etching mask to etch through the thick parylene-C layer as is shown in FIG. 1D. Finally, electrode sites **170**, **175** and device contour **180** are defined by reactive ion etching (such as a 2-step O₂ plasma etching as is shown in FIG. 1E) or deep reactive ion etching (DRIE) can be used.

Although the foregoing example uses parylene-C, the processes and embodiments of the device herein are not so limited. Other parylenes such as parylene N, C, D, HT, AM, A or combinations thereof can also be used. Parylene-C is the preferred parylene. Although parylene is the preferred substrate, a skilled artisan will appreciate that the material can be other thin-film polymers such as polyimide, Teflon, Kapton, or a printed circuit board (PCB) and the like.

Other materials useful for substrate and/or carrier design include, but are not limited to, silicon, glass, steel, G10-FR4, or any other FR4 family epoxy, etc. In some embodiments, the silicon substrate is used only as a carrier during fabrication and is accordingly removed before the package is complete. In other embodiments, the carrier remains an integral part of the package.

In certain aspects, the silicon-wafer used in the methods is treated with 1,1,1,3,3,3-hexamethyldisilazane (HMDS). A skilled artisan will appreciate other treatments can be used to release the parylene structure from the silicon wafer.

In certain aspects, the first parylene layer **120** and the second parylene layer **150** are deposited on the silicon substrate by chemical vapor deposition (CVD). The first layer has a thickness of between about 0.1 μm to about 100 μm thick such as 10, 20, 30, 40, 50, 60, 70, 80, 90, or 100 μm. Preferably, the thickness of the first parylene layer (bottom layer) is between about 1 μm and about 10 μm thick such as about 1, 2, 3, 4, 5, 6, 7, 8, 9, or 10 μm thick.

Typically the second parylene layer (top layer) **150** is thicker than the first parylene layer **120**. In one instance, the second parylene layer is between 10 μm and 200 μm thick such as 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150, 160, 170, 180, 190 or 200 or even thicker. Preferably, the second parylene layer is between 20 μm and 60 μm thick such as about 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59 or 60 μm thick.

In certain aspects, the metal **130** used for the lift-off is a titanium/gold (Ti/Au) alloy. However, other suitable metals and alloys include, but are not limited to, Cr/Au, Ni/Au, Ti/Au, Al/Ti, Ag/Ti, Cr/Au/Ti/Ni/Au, Ni/Pd/Au, Ti/Ni/Au or combinations thereof. Those of skill in the art will know of other metals useful for the present invention.

The process includes providing a mask such as a metal mask deposited as a parylene-C etching mask to etch through the second parylene-C layer. In general, etching is a reactive ion etching (RIE) masked by a metal mask. In addition, deep reactive etching can be used (DRIE). Other suitable mask materials are also useful. The RIE can be oxygen plasma etching.

A skilled artisan will appreciate that the parylene layers of the parylene devices described herein are not limited to two parylene layers. In addition, the metal of the parylene device is not limited to a single metal. The parylene devices are based on a sandwich structure. As long as a metal is sandwiched by a top and a bottom parylene layer, there can be numerous layers stacked on the substrate. In addition, there can be a plurality of masks to open the electrodes and define the contour of the device(s).

In certain instances, the process described is used to generate multiple parylene-metal-parylene sandwich layers on a

6

carrier (e.g., a silicon wafer) such as a plurality of sandwich layers including 2, 3, 4, 5, 6, 7, 8, 9, 10 or more parylene-metal-parylene sandwich layers. Although the process just described generates 1 sandwich layer, a skilled artisan will appreciate that the process can be repeated to make any number of sandwich layers.

In still other aspects, the invention includes a parylene substrate made by the processes herein. As is described in more detail below, the invention provides attaching a device to the parylene substrate such device includes, for example, an integrated circuit and other discrete components.

In certain aspects, the inventive thin-film (e.g., parylene) substrate hosts electronic components such as application specific integrated circuits (ASICs), which are interconnected via metallization traces, such as about 3.7 μm wide metallization trace. In one embodiment, the fabricated flexible parylene-C substrate is connected with an IC chip and other discrete components. In certain other aspects, the substrate or micro-module of the present invention contains a variety of components including, but not limited to, one or more integrated circuits, ASICs, interconnect layers, heat sinks, conductive vias, passive devices, MEMS devices, sensors, pre-manufactured electrical components, transistors, resistors, capacitors, inductors, micropumps and filters. The components are arranged and stacked within the module in a wide variety of different ways. The layers and components of the module can be deposited and processed using various conventional wafer level processing techniques, such as spin coating, lithography and/or electroplating.

The parylene package can include many other types of devices and components than the ones illustrated. The package can also contain almost any number of active and/or passive devices. Examples of such active and/or passive devices includes resistors, capacitors, oscillators, magnetic cores, MEMS devices, sensors, cells, communication devices, integrated thin film battery structures, inductors, and the like. These devices can be positioned and/or stacked in various locations within the package. The components may take the form of prefabricated discrete components or may be formed in-situ. One advantage of the lithography-based process used to create the present package is that these and other components can be formed in-situ during the layered formation of the package. That is, while prefabricated, discrete components can be placed in almost any position within package, components can also be fabricated directly onto any photo-imageable layer using any suitable technique, such as conventional sputtering and/or electroplating.

Turning now to FIG. 2A, a schematic representation **200** is shown of the fabricated flexible parylene-C substrate **210** connected with an integrated chip **220** and discrete components e.g., capacitor **211** and oscillator **217**. In certain aspects, the multi-electrode array **230** with outputs **232** is placed on the macula of a human eye or an eye of another mammal and can be fixed by a retinal tack **235** (FIG. 2D). In one instance, integrated discrete components are placed on or in an eyeball. FIG. 2B is the backside of the discrete component area. FIG. 2C shows a close-up view of the chip integration. FIG. 2E is a schematic of an eye showing positioning of an electrode array **241**, integrated ASICs **245** and an intraocular RF coil **250**.

As shown in FIG. 2A, the discrete components such as for example a capacitor **211** and an oscillator **217** are mounted and connected by conductive epoxy to make an electrical connection. In certain instances, two incisions or suture holes are made for the device to be fixed in an eyeball **261**, **265** (see, FIG. 2E). In one aspect, a multi-electrode array **230** is placed on the macula and fixed by a retinal tack **235**. FIG. 2E also

shows the electrode array **241**, inside one incision **261** and the integration of the application specific integrated circuit **245** in the other incision **265**. An intraocular RF coil **250** is also shown. The interconnection part is preferably about 0.1 mm to about 6 mm wide such as about 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1, 2, 3, 4, 5, or 6 mm wide. In certain instances, the interconnection is about 2 mm wide. In certain instances, the interconnection depends on the incision size for surgery on the eyeball. However, in most instances, the width is about 2 or 3 mm.

In certain instances, IC chips having high-density and multi-channel bonding pads (e.g., pad size smaller than about 100 $\mu\text{m} \times 100 \mu\text{m}$; pitch smaller than about 200 μm) can be connected with a parylene substrate by a conductive epoxy squeegee technique. Other discrete components with larger bonding pads, such as caps and oscillators, can be connected with a parylene substrate manually by conductive epoxy using needles. Power and data coils with larger bonding pads can also be connected with a parylene substrate manually by conductive epoxy using needles. The whole integrated device is then fixed inside an eyeball by a retinal tack (e.g., close to electrode array).

In another embodiment, the present invention provides methods for integrating the flexible parylene substrate with an IC chip and other discrete components. The method includes chip pattern lithography, including photoresist spinning, baking, exposing, and developing as well as integrating the IC chip into the flexible parylene substrate. As shown in FIG. 3A, IC chip assembly can be done in a custom holder **300**.

In operation, chips **310**, **315**, **320** are first secured in a holder **300**, and all the chip pattern lithography, including photoresist spinning, baking, exposing, and developing is done in this holder in series. After chip integration with a parylene-C interface by a conductive epoxy squeegee connection, the chip **315** can be released from the back side of the mold, which is beneficial for the whole device to be implanted inside the eyeball. The chip can be integrated and packaged into the flexible parylene substrate. The processing of the IC chips to form a patterned IC chip is typically done on a custom chip pattern mold. FIG. 3A also shows the mold can serve as a safety buffer zone for a squeegee process. The size and the depth of the mold is designed to accommodate various sizes of the chip. FIG. 3B shows an expanded view of an IC chip.

In one example of a squeegee process of the present invention, a commercially available conductive epoxy is first mixed well and applied on the surface of an edge of the parylene substrate. In certain instances, the parylene substrate has pre-designed holes and/or wells that are etched during the fabrication process. The holes and/or wells serve as a screen for this process after the IC chip is aligned and bonded well with the parylene substrate. A rubber squeegee is then used to push the epoxy across the surface, so the epoxy fills the holes and/or wells in the parylene substrate, to electrically connect the parylene substrate and IC chip.

In certain instances, dummy chips with conductive traces are fabricated to simulate the actual chip and special pads are pre-connected for connection yield measurement. For example, FIG. 4A shows a dummy chip for an assembly yield test. FIG. 4B shows pads can also serve as alignment marks. FIG. 4C shows a metal pad exposed with a resolution of around 5 μm being achieved.

The present invention provides methods and processes for a low-temperature bonding between a thin-film (e.g., parylene such as parylene C) and silicon using photo-patternable adhesives. This method can be used to determine the bonding pads and also reduce the residual stress in packaging. Advantageously, this low-temperature bonding allows selec-

tively local area bonding, without applying a high electric field. Thus it is especially suitable for the integration of a parylene substrate with microelectronics in MEMS packaging.

As such, in yet another embodiment, the present invention provides a method for assembling an integrated circuit to a thin-film substrate. Although parylene is the preferred substrate, a skilled artisan will appreciate that the material can be other thin-film polymers such as polyimide, Teflon, kapton, or a printed circuit board (PCB) and the like. The method comprises:

- spin coating a photo-patternable adhesive or epoxy to an integrated circuit (IC) to form a covered IC;
- masking the covered IC; and
- 15 patterning the covered IC using photolithography to expose a plurality of bonding pads on the IC to form a patterned IC, for integration into a thin-film (e.g., parylene) substrate.

In certain instances, the invention provides low-temperature bonding processes to facilitate the connection and packaging of various components for use as biomedical implants. In certain instances, the bonding technology can be used to facilitate the connection between parylene-C substrates and an IC as well as discrete components, which substrates have pre-metalized electrical connections. The chips are preferably bound on the substrates with proper alignment so the metal pads on the parylene substrates and the metal pads on the chips line up.

In certain instances, commercially available photo-patternable materials such as photo-patternable adhesive or epoxy can be used. In certain aspects, the photo-patternable material is a photoresist. Suitable photoresist includes SU-8, AZ4620, AZ1518, AZ4400, AZ9260, THB-126N, WPR-5100, BCB, polyimide and the like. The processing conditions are facile with respect to bonding temperature, pressure, time, and surface treatment. The results show that for example, the epoxy-based SU-8 is very effective with a peeling force up to 6.3N.

In certain instances, AZ4620 photoresist is used in the processes due to excellent reflow properties (P. J. Chen et al., *J. Microelectromech. Syst.*, 17 (2008), pp. 1352-1361). The patterned AZ4620 photoresist is baked at 100° C. to about 180° C. such as 140° C. for 10 minutes to 80 minutes such as about 30 minutes in vacuum oven and its smooth surface formed by reflow helps the conductive epoxy refill, as shown in FIG. 5A-D. The side lengths were almost the same before and after baking such that the reflow photoresist does affect conductivity by covering the whole metal pad. In one specific embodiment, in no way limiting, FIG. 5A illustrates unbaked AZ4620. FIG. 5B shows AZ4620 baked at 140° C. for 30 minutes in a vacuum oven. FIGS. 5C and 5D show that the slope formed by reflow is beneficial for conductive epoxy to be fed through. Advantageously, the side lengths show no change before and after baking.

In previous applications, conductive epoxy was fed through the cavity embedded in a parylene-C substrate and relied on to make both electrical and mechanical connections. As shown in FIG. 6A, the prior art process uses only conductive epoxy **615** to connect the parylene substrate and the chip **602**. The metal pad is shown as **625**. In the process of the present invention, both conductive epoxy **615** and photo-patternable adhesive (e.g., photoresist) **610** such as AZ4620 is used. In fact, after applying AZ4620 (as glue here) to the chip **602**, the total gluing area between parylene-C substrate and a chip **602** is increased from 2% to 94%, as shown in FIG. 6B. In certain instances, the unnecessary pads were also covered to avoid shortage happening underneath the parylene-C interface during a squeegee connection process.

The high-density connections between the chip and the parylene-C substrate were again done by conductive epoxy squeegee, while the custom holder provided the safety buffer zone for squeegee to totally replace the function of PDMS holders (see, Jay H. C. Chang, Ray Huang, and Y. C. Tai, *Proc. NEMS* 2011, pp. 1110-1113).

II. Low-Temperature Bonding Between Parylene-C and Silicon

In certain instances, the photo-patternable adhesives are first spin-coated on clean silicon wafers with for example, HMDS and oxygen plasma treatments, followed by standard photolithography process to define the bonding pads. In certain preferred aspects, the methods include baking the patterned IC to form a smooth surface. In certain other instances, the parylene substrate is first treated with oxygen plasma to enhance bonding with photo-patternable adhesives. In still other instances, the IC chip is treated by HMDS and/or oxygen plasma to enhance bonding with photo-patternable adhesives.

Focusing on the application on chip integration, as an illustrative example of photo-patternable adhesives, SU-8 (13 μm and 28 μm), and AZ4620 (10 μm and 19 μm) are selected as an illustration to create suitable aspect ratios of the cavity or opening. Other photoresists include AZ1518, AZ4400, AZ9260, THB-126N, WPR-5100, BCB, polyimide and the like.

As is shown in FIG. 7, a clean 30 μm parylene-C film 730 treated by oxygen plasma is then aligned with a diced wafer 740 and the structure is sandwiched by two glass slides 715, 725. A clamp 750 having two arms 710, 720 is used as a bonding tool to make good contact and apply constant force on the testing samples. The heating process is operated in a vacuum oven and the maximum testing temperature is set to be about 120-180° C. such as about 150° C. to prevent damage to the IC chips.

FIGS. 8A and 8B show one example of cross-sectional SEM images of samples bonded by photo-patternable adhesives. The bonding pads are well defined with desired thickness and the shape of the microstructures is not changed during the bonding process. Moreover, the flexible intermediate adhesives does not cause residual stress after bonding.

In one aspect, the methods include first treating the parylene substrate with oxygen plasma treatment to enhancing bonding. Such plasma treatment conditions include, for example, about 10 W to about 100 W such as about 50 W; 100 mtorr to about 300 mtorr such as about 200 mtorr; and 0.1 minute to about 5 minutes such as about 1 minute duration.

In certain instances, each of the plurality of bonding pads is between 1 μm and 10 μm . In certain instances, the bonding pads can each be different dimensions. The thickness of photo-patternable adhesives on the IC chip is from 10 μm to 30 μm such as 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29 or 30 μm . In certain instances, the patterned IC and a parylene substrate are assembled using conductive epoxy or paste. The methods include delivering conductive epoxy to make a high-density multi-channel IC chip connection by a high-throughput squeegee technique. In certain instances, the high-density multi-channel IC chip is greater than 1000 channels on a 25 mm^2 chip area or even 10,000 channels on a 36 mm^2 or about 5-300 channels per mm^2 chip area.

In certain aspects, when IC chips have a pitch size larger than about 200 μm , applying conductive epoxy is performed with needles having a diameter smaller than 100 μm . As discussed above, the process on IC chips to form a patterned

IC chip is done on a custom chip pattern mold. The mold serves as a safety buffer zone for the squeegee process. The size and the depth of the mold are designed to accommodate the size of the chip.

As is shown in FIG. 9A, the peeling force is measured by a force gauge setup to investigate bonding strength. FIG. 9B shows a testing sample after bonding; FIG. 9C shows a schematic representation of the testing sample.

Each data point represents the average of five measurements. Force gauge is fixed on a motorized stage to pull the partially peeled film at 90 degree with a speed of 100 $\mu\text{m/s}$. Peeling force as a function of bonding temperature is shown in FIG. 10.

FIG. 11 shows peeling force as a function of bonding pressure. After analysis, the results show that the higher the bonding temperature and pressure, the stronger the bonding.

Advantageously, parylene-C film treated by oxygen plasma dramatically enhances the bonding for photo-patternable adhesive such as photoresists (e.g., SU-8) (see, Blanco F J et al., *J. Micromech. Microeng.* 14 (2004), 1047-1056). SU-8 microstructure will not deform even under bonding pressure of 2 MPa where the maximum bonding forms. FIG. 12A shows the maximum peeling force of different photopatternable adhesives. FIG. 12B shows the peeling force versus bonding time for different photo-patternable adhesives. Z4620 can withstand pressure up to 0.5 MPa. In certain aspects, the bonding time has almost no effect on the bonding strength when the samples are heated more than one hour.

As a demonstration, this technique is applied on a 268-channel conduction chip integrated with parylene-C surgical device for retinal implant (FIG. 13). After patterning the adhesives on chips (see, J. H. Chang et al, *Proc. MEMS* 2012, pp. 353-356), the spatial resolution of bonding pads built by SU-8 can be 5 μm . The bonding area is increased from 2% to 94% and the measured connection yield is improved from 92% to 98%.

This low-cost and low-temperature bonding process is proven to enable the sealing of MEMS structures.

In another embodiment, the present invention provides a biocompatible thin-film substrate. Although parylene is the preferred substrate, a skilled artisan will appreciate that the material can be other thin-film polymers such as polyimide, Teflon, kapton, or a printed circuit board (PCB) and the like. The invention provides a thin-film (e.g., parylene) substrate for attachment of a device, comprising:

- a first thin-film (e.g., parylene) layer;
- a metal adjacent to the first thin-film (e.g., parylene) layer;
- a second thin-film (e.g., parylene) layer adjacent to the metal to form a thin-film metal thin-film (e.g., parylene-metal-parylene) sandwich, wherein the second layer of parylene has an opening or cavity, the opening having at least one electrical contact provided on an internal surface thereof, the opening configured to accept at least one electrical circuit device and to provide electrical communication between the at least one electrical contact and the at least one electrical circuit device, said biocompatible thin-film (e.g., parylene) substrate configured to be implanted within a living organism after accepting the at least one electrical circuit device.

In certain aspects, the device having at least one electrical circuit is an integrated circuit (IC) chip. In addition, the device such as an IC chip is integrated in the substrate by a conductive epoxy squeegee electrical connection. Preferably, the device is integrated into the substrate by a photo-patternable adhesive used as a mechanical glue. In one embodiment, the whole structure (e.g., the device having at least one electrical circuit is an integrated circuit (IC) chip) is conformally coated and sealed with parylene-C (poly-para-xylylene-C), and if necessary, with medical grade epoxy to achieve total encapsulation for biocompatibility.

In certain instances, once the device is implanted, there can be communication with the implanted device and an external device. Communication can be performed using either percutaneous connectors or wireless communication methods. Some of the kinds of signals that are communicated between the implanted device and an external device include power signals and data signals. Power signals can include signals that provide power from an external power supply to an implanted device, so that a battery present in the implanted device can be maintained in a suitable state of charge, or so that a battery can be eliminated from the implanted device. For some conventional devices having batteries, surgery may become necessary to replace the device because its battery is expected to reach the end of its useful life. Any surgery poses a health risk and unnecessary surgery is best avoided if possible, especially in persons who already have health issues. Accordingly, implantable devices that do not have to be replaced because of a battery are advantageous.

Data signals can include data signals from an external detector to an implanted device (such as providing an electrical signal corresponding to an audible signal received by a microphone to a cochlear implant for communication by way of a person's nervous system to the person's brain), control signals from an external detector to an implanted device that provide the ability to control the implanted device by using such signals (e.g., controlling the state of operation of the implanted device to meet the needs of the person), and data signals from the implanted device to an external device to monitor the condition and operation of the implanted device itself, to monitor the condition of the person (such as pulse rate, cardiac signals, or other signals relating to the condition being treated) and conditions in the vicinity of the implanted device (such as physiological signals, e.g., temperature, pressure, pH), or to monitor the signals the implanted device is applying to the person. In some embodiments, data signals can be used to "tune" or "reprogram" the implanted device to take advantage of improvements in understanding of the person's condition and the intervention, assistance, or treatment that the person should have, or provide improvements in the implantable device operation and control procedures or operational software that are developed after the device is implanted.

Additional integrated circuits within package or module can be arranged in a wide variety of ways and may be placed at other location within the package. By way of example, different integrated circuits may be positioned in different photo-imageable layers and/or within the same layer. In various embodiments, the integrated circuits can be stacked, positioned side-by-side, placed in close proximity to one another and/or be separated by a substantial distance relative to the overall size of package. Integrated circuits can also have a variety of different form factors, architectures and configurations. For example, they may take the form of relatively bare dice (e.g., unpackaged dice, flip chips etc.), or partially and/or fully packaged dice.

III. Device Testing

The following operational tests illustrate the reliability experiments to test the electrical connections of the parylene substrate.

FIG. 14 illustrates the setup 1400 for the test measurements. As shown therein, the electrode array outputs 1410, 1415 were probed to check the electrical connections. In certain aspects, these electrodes are placed on the macula of a mammalian eye such as a human eye.

The setup 1400 includes a patterned chip 1428 and a parylene interface 1433. Photoresist 1420 is sandwich between the wafer 1428 and the parylene 1430. In addition, metal 1425 is included between the wafer 1428 and the photoresist 1420, or between the conductive epoxy 1418 and the wafer. Electrically conductive vias are provided to electrically connect components (e.g., ICs/traces/contacts/passive components, etc.) that reside at different layers of the package. The vias are arranged to extend through various layers. By way of example, the vias may be used to couple traces from two different interconnect layers together; a die or another component to an interconnect layer; a contact to a trace, die or other component, etc.

In one experiment, the connection yield right after squeegee was measured by probing using 1440 and 1441, the stimulating electrodes. Afterwards, an additional thick parylene-C was coated on the entire device (except the output electrodes) to insulate and stabilize the connection, and to protect the metals embedded in the parylene-C substrate from corrosive body fluids. The connection yield was recorded after this coating. Finally, the device was soaked in 90° C. saline solution for 5 days and the connection yield was again recorded.

The results in FIG. 15 show that the yield in operation of the inventive device under four different conditions. Reliability tests were carried out after squeegee connection; soaking without encapsulation; encapsulation by parylene-C coating; and accelerated soaking in 90° C. saline. The results indicated that the processes combined with thick parylene-C coating for packaging does provide a high connection yield.

The results indicate that the new gluing technique is satisfactory (~98%), while the yield without the new technique is significantly lower (~88%). Moreover, for the connections without photoresist gluing techniques, most of the disconnections happened at peripheral pads where delamination force is applied.

In addition, the limits of the pad size and separation between pads were investigated. Chips with different pad separations and sizes were designed and fabricated for measurement.

FIG. 16A shows chips with 40 μm by 40 μm pad size and 40 μm separation. FIG. 16B shows connections between parylene substrate and a chip. FIG. 16C shows yield vs separation of pads. FIG. 16D shows yield vs side length of pads. The results show that high connection yield (>90%) can be achieved for pads as small as 40 μm by 40 μm and with a 40 μm separation in between.

Based on these current results, as many as 10,000 connections within an area of 6 mm by 6 mm is achieved. This is satisfactory for current retinal prosthetic applications.

It is understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims. All publications, patents, and patent applications cited herein are hereby incorporated by reference in their entirety for all purposes.

What is claimed is:

1. A method for fabricating a flexible thin-film substrate for attachment of a device to be implanted, the method comprising:

- depositing a first thin-film layer on a silicon-wafer to form a bottom thin-film layer;
- depositing a metal to the bottom thin-film layer to form an electrical connection;

13

- depositing a second thin-film layer adjacent to the metal to form a top thin-film layer and to thereby form a thin-film metal thin-film sandwich;
- providing a mask adjacent to the second thin-film layer; directing an etching beam onto the mask to fabricate the flexible thin-film for attachment of the device,
- detaching the silicon-wafer from the flexible thin-film substrate and attaching the device, wherein the device is an integrated circuit chip (IC Chip), which electrically connects the flexible thin-film substrate to the IC Chip, and wherein the flexible thin-film substrate and device are encapsulated for biocompatibility.
2. The method of claim 1, wherein the first thin-film layer and the second thin-film layer are each independently selected from the group consisting of parylene, polyimide, polytetrafluoroethylene (PTFE), poly (4,4'-oxydiphenylene-pyromellitimide) and a printed circuit board (PCB).
3. The method of claim 2, wherein the first thin-film layer and the second thin-film layer are each parylene.
4. The method of claim 3, wherein the parylene is a member selected from the group consisting of parylene N, parylene C, parylene D, parylene HT, parylene AM, parylene A and combinations thereof.
5. The method of claim 4, wherein the parylene is parylene C.
6. The method of claim 1, wherein the silicon-wafer is treated with 1,1,1,3,3,3-hexamethyldisilazane (HMDS).
7. The method of claim 3, wherein the first parylene layer is deposited by chemical vapor deposition (CVD).

14

8. The method of claim 3, wherein the first parylene layer is between 0.1 μm and 100 μm thick.
9. The method of claim 8, wherein the first parylene layer is between 1 μm and 10 μm thick.
10. The method of claim 1, wherein the metal is a conductor selected from the group consisting of Cr/Au, Ni/Au, Ti/Au, Al/Ti, Ag/Ti, Cr/Au/Ti/Ni/Au, Ni/Pd/Au, and Ti/Ni/Au.
11. The method of claim 10, wherein the metal is Ti/Au.
12. The method of claim 3, wherein the second parylene layer is deposited by chemical vapor deposition (CVD).
13. The method of claim 12, wherein the second parylene layer is between 10 μm and 200 μm thick.
14. The method of claim 13, wherein the second parylene layer is between 20 μm and 60 μm thick.
15. The method of claim 3, wherein the etching is reactive ion etching (RIE) masked by a metal mask.
16. The method of claim 3, wherein the etching is deep reactive ion etching (DRIE) masked by a metal mask.
17. The method of claim 15, wherein the RIE is oxygen plasma etching.
18. The method of claim 3, wherein the parylene, metal, parylene deposition steps are repeated to generate a plurality of parylene-metal-parylene sandwich layers.
19. The method of claim 1, wherein the device is integrated with the substrate with an epoxy squeegee connection.
20. The method of claim 1, wherein the substrate and the device is encapsulated in parylene C.

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